What is claimed is:

1. A direct-conversion transmitting circuit, characterized by local modulation circuit comprising first and second mixers, and first and second low-pass filters, first and second gain/bias adjustment means, and a first phase shifter, wherein high frequency output terminals of said first and second mixers are connected to each other; an output terminal of said first low-pass filter is connected to an input terminal of said first mixer; the input terminal of said first low-pass filter is connected to an output terminal of said first gain/bias adjustment means; the output terminal of the second low-pass filter is connected to an input terminal of the second mixer; the input terminal of the second low-pass filter is connected to an output terminal of said second gain/bias adjustment means; a first output terminal of said first phase shifter is connected to a local signal input terminal of said first mixer; a second output terminal of said first phase shifter is connected to a local signal input terminal of said second mixer; and input signals are applied to an input terminal of said first gain/bias adjustment means and an input terminal of said second gain/bias adjustment means, respectively.

2. A direct-conversion transmitting circuit according to claim 1, characterized in that said phase shifter is composed of a frequency divider circuit.

3. A direct-conversion transmitting circuit according to claim 1, characterized in that each circuit of said first and second low-pass filters is composed of a filter whose order is

at least a second order.

4. A direct-conversion transmitting circuit according to claim 3, characterized in that said first and second low-pass filter circuits are each composed of a Sallen-Key type filter circuit,

the Sallen-Key type filter is composed of first and second resistors, first and second capacitors, and a first transistor, and

a first terminal of said first resistor is an input of the filter; a second terminal of said first resistor is connected to a first terminal of said second resistor; a second terminal of said second resistor is connected to a base of the first transistor; a first terminal of said first capacitor is connected to the second terminal of said first resistor; a second terminal of said first capacitor is connected to an emitter of said first transistor; a first terminal of said second capacitor is connected to the second terminal of said second resistor; a second terminal of said second capacitor is connected to a grounding potential; a collector of said first transistor is connected to a power source potential; and an emitter of said first transistor is an output terminal of the filter.

5. A direct-conversion transmitting circuit according to claim 3, characterized in that each of said first and second low-pass filter circuits is composed of two sets of first and second Sallen-Key type filter circuits,

said first and second Sallen-Key type filter circuits are

each composed of a first, second, third, and fourth resistors, a first and second capacitors, and a first and second transistors,

a first terminal of said first resistor is an input terminal of said filter circuit; a second terminal of said first resistor is connected to a first terminal of said second resistor; a second terminal of said second resistor is connected to a base of said first transistor; a first terminal of said first capacitor is connected to the second terminal of said first resistor; a second terminal of said first capacitor is connected to an emitter of said first transistor; a first terminal of said second capacitor is connected to the second terminal of said second resistor; a second terminal of said second capacitor is connected to a grounding potential; a collector of said first transistor is an output terminal of said filter circuit; a first terminal of said third resistor is connected to the emitter of said first transistor; a second terminal of said third resistor is connected to a grounding potential; a collector and a base of said second transistor are connected to the first terminal of the first resistor; a first terminal of said fourth resistor is connected to an emitter terminal of said second transistor; and a second terminal of said fourth resistor is connected to a grounding potential,

each of said first and second gain/bias adjustment means is composed of: a first differential pair serving as a voltage/current converter circuit that converts a differential voltage into a differential current; and a second and third

differential pairs comprising a first and second collector output terminals, a first and second base input terminals, and an emitter coupling input terminal, and

a first collector output terminal of said first differential pair is connected to said input terminal of said first Sallen-Key filter circuit; a second collector output terminal of said first differential pair is connected to an input terminal of said second Sallen-Key filter circuit; an output terminal of said first Sallen-Key filter circuit is connected to an emitter coupling input terminal of said second differential pair; an output terminal of said second Sallen-Key filter circuit is connected to an emitter coupling input terminal of said third differential pair; first collector output terminals of said second and third differential pairs are connected to each other; second collector output terminals of said second and third differential pairs are connected to each other; a second base input terminal of said third differential pair is connected to a first base input terminal of said second differential pairs; and a first base input terminal of said third differential pair is connected to a second base input terminal of said second differential pair.

6. A direct-conversion transmitting circuit according to claim 1, characterized in that said first and second mixers are each composed of a differential circuit, and input terminal pairs of said first and second mixers are provided with a first and second DC offset correction circuits to which output terminal pairs are connected,

each of said first and second DC offset correction circuits is composed of a control means having a DA converter, an AD converter, and two outputs,

one output of said control means is connected to an input terminal of said DA converter; the other output of said control means is connected to an input terminal of said AD converter; respective output pairs of said DA converter and said AD converter are connected to each other and thereby are said output terminal pairs, and

the control means operates said DA converter before the direct-conversion transmitting circuit generates a signal, converts the signal to a logical signal in accordance with a magnitude of a DC component generated at each input terminal of said first and second mixers, and has a function of generating, from said AD converter, a DC level for offsetting the DC component on the basis of a value of the logical signal and a function of storing an optimal level converted into said logical signal.

7. A direct-conversion transmitting circuit according to claim 1, characterized in that the direct-conversion transmitting circuit is composed of: a first and second control means each having a first and second DA converters, an AD converter, and two outputs; a DC offset correction circuit having a first, second, third and fourth output terminals pairs; and further a switching means having two sets of output terminal pairs,

an output of said first control means is connected to an

input of said first DA converter; an output of said second control means is connected to an input of said second DA converter; an output pair of said first DA converter is connected to a first output terminal pair of said DC offset correction circuit; an output pair of said second DA converter is connected to a second output terminal pair of said DC offset correction circuit; and an output of said AD converter is connected to a third output terminal pair of said DC offset correction circuit,

said first and second mixers each are composed of a differential circuit, in which the first output terminal pair of said DC offset correction circuit is connected to an input terminal pair of said first mixer; the second output terminal pair of said DC offset correction circuit is connected to an input terminal pair of said second mixer; and the third output pair of said DC offset correction circuit is connected to an input terminal pair of said switching means,

one output terminal pair of said switching means is connected to the input terminal pair of said first mixer; and the other output terminal pair of said switching means is connected to the input terminal pair of said second mixer, and

each of said first and second control means operates said first and second DA converters before the direct-conversion transmitting circuit generates a signal, and converts the signal to a logical signal based on magnitude of a DC component generated at input terminals of said first and second mixers, and has a function of switching said switching means such that

a DC level generated by said AD converters is applied to the input terminal pairs of said first and second mixers at a different period in order to offset a DC component generated at each of the input terminal pairs of said first and second mixers in accordance with a value of the logic signal, and a function of storing an optical level converted into said logical signal.

8. An integrated transmitting/receiving circuit including a transmitting section and a receiving section which are integrated on the same chip, wherein the transmitting section is composed of a first direct-conversion transmitting circuit using the direct-conversion transmitting circuit according to claim 1, and a third and fourth amplifiers, and wherein the receiving section is composed of a first to third low noise amplifiers, a third and fourth mixers, a first to third frequency dividers, a first frequency synthesizer, a first voltage control type oscillator, and a first and second baseband frequency amplifiers/filter rows,

the integrated transmitting/receiving circuit characterized in that an output of said first direct-conversion transmitting circuit is connected to respective input circuits of said third and fourth amplifiers; said third and fourth amplifiers are used as independent output terminals; input terminals of said first to third low noise amplifiers are connected to one another to connect inputs of said third and fourth mixers; outputs of said third and fourth mixer circuits are connected to said first and second baseband frequency

amplifiers/filter rows; a first output of said first frequency divider is connected to a local signal input terminal of said third mixer; a second output of said first frequency divider is connected to a local signal input terminal of said fourth mixer circuit; an output terminal of said first frequency synthesizer is connected to a control voltage input terminal of said first voltage control oscillator; an output of said first voltage control oscillator is connected to an input of said first frequency synthesizer; an output of said first voltage control oscillator is connected to an input terminal of said second frequency divider having two functions of executing and bypassing a frequency dividing function; said second frequency divider is connected to an input of said first frequency divider; an output of said first voltage control oscillator is connected to an input terminal of said third frequency divider having two functions of executing and bypassing a frequency dividing function; said third frequency divider is connected to an input terminal of a first phase shifter in said first direct-conversion transmitting circuit, and said first phase shifter is a frequency shifter.

9. An integrated transmitting/receiving circuit according to claim 8, characterized in that a fourth frequency divider is interposed between said second and third frequency dividers whose respective input terminals are connected to the input terminal of said first voltage control frequency.

10. An integrated transmitting/receiving circuit according to claim 9, characterized in that said fourth

frequency divider has two functions of executing and bypassing a frequency dividing function, and

a fourth low noise amplifier is further provided whose an input terminal is independent from respective input terminals of the other low noise amplifiers and whose an output terminal is connected to respective output terminals of the other low noise amplifiers.